WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

an internal circuit having first and second external terminals;

first and second fuse elements, each having first and second terminals, the first terminals of the first and second fuse elements being respectively connected to the first and second external terminals; and

a discharge line connected to the second terminals of the first and second fuse elements and serving as an electrostatic discharge current path.

2. The semiconductor integrated circuit according to claim 1, wherein:

the internal circuit further has a MOS transistor having a gate connected to the first external terminal; and

each of the first and second fuse elements has a resistance value that satisfies:

$$V_{OX} > (R_m + R_x) \times I_{esd}$$

where V_{OX} represents a breakdown voltage of a gate oxide film of the MOS transistor, R_m represents a wire resistance value in the electrostatic discharge current path between the first and second external terminals, R_x represents a resistance value of all fuse elements arranged in the electrostatic discharge current path between the first and second external terminals, and I_{esd} represents a value of an electrostatic discharge

current.

3. The semiconductor integrated circuit according to claim 1, wherein the fuse elements remain firm even when energy of 200μJ is applied thereto.

4. The semiconductor integrated circuit according to claim 1, wherein the fuse elements remain firm even when energy of 200μJ is applied thereto but break when a direct current of 30mA is applied thereto within 20 seconds.

5. The semiconductor integrated circuit according to claim 1, wherein the fuse elements are electrically disconnected when the semiconductor integrated circuit is mounted on a circuit board.

6. A semiconductor integrated circuit comprising:

an internal circuit having first and second external terminals;

an electrostatic protecting circuit connected to the second external terminal;

a fuse element having first and second terminals, the first terminal of the fuse element being connected to the first external terminal; and

a discharge line connected to the electrostatic protecting circuit and the second terminal of the fuse element and serving as an electrostatic discharge current path.

7. The semiconductor integrated circuit according to claim 6, wherein:

the internal circuit further has a MOS transistor having a gate connected to the first external terminal; and

the fuse element has a resistance value that satisfies:

$$V_{OX} > (R_m+R_x) \times I_{esd}$$

where V_{OX} represents a breakdown voltage of a gate oxide film of the MOS transistor, R_m represents a wire resistance value in the electrostatic discharge current path between the first and second external terminals, R_x represents a resistance value of the fuse element, and I_{esd} represents a value of an electrostatic discharge current.

8. The semiconductor integrated circuit according to claim 6, wherein the fuse element remains firm even when energy of 200μJ is applied thereto.

9. The semiconductor integrated circuit according to claim 6, wherein the fuse element remains firm even when energy of 200μJ is applied thereto but breaks when a direct current of 30mA is applied thereto within 20 seconds.

10. The semiconductor integrated circuit according to claim 6, wherein the fuse element is electrically disconnected when the semiconductor integrated circuit is mounted on a circuit board.

11. A semiconductor integrated circuit comprising:

an internal circuit having first, second and third

external terminals;

a fuse element having first and second terminals, the first terminal of the fuse element being connected to the first external terminal;

first and second electrostatic protecting circuits respectively connected to the second and third external terminals;

a first discharge line connected to the first and second electrostatic protecting circuits and serving as an electrostatic discharge current path; and

a second discharge line connected to the second terminal of the fuse element and the second external terminal and provided to keep the first and second external terminals at substantially the same potential.

12. The semiconductor integrated circuit according to claim 11, wherein:

the internal circuit further has a MOS transistor having a gate connected to the first external terminal; and

the fuse element has a resistance value that satisfies:

$$V_{OX} > (R_m+R_x) \times I_{esd}$$

where V_{OX} represents a breakdown voltage of a gate oxide film of the MOS transistor, R_m represents a wire resistance value in the electrostatic discharge current path between the first and second external terminals or between the first and third external terminals, R_x

represents a resistance value of the fuse element, and I_{esd} represents a value of an electrostatic discharge current.

13. The semiconductor integrated circuit according to claim 11, wherein the fuse element remains firm even when energy of 200μJ is applied thereto.

14. The semiconductor integrated circuit according to claim 11, wherein the fuse element remains firm even when energy of 200μJ is applied thereto but breaks when a direct current of 30mA is applied thereto within 20 seconds.

15. The semiconductor integrated circuit according to claim 11, wherein the fuse element is electrically disconnected when the semiconductor integrated circuit is mounted on a circuit board.

16. A semiconductor integrated circuit comprising:

a digital circuit having a first external terminal;

a first electrostatic protecting circuit connected to the first external terminal;

a first discharge line connected to the first electrostatic protecting circuit and serving as an electrostatic discharge current path;

an analog circuit having a second external terminal;

a second electrostatic protecting circuit connected to the second external circuit;

a second discharge line connected to the second electrostatic protecting circuit and serving as an electrostatic discharge current path; and

a fuse element connected between the first and second discharge lines and serving as an electrostatic discharge current path of the digital and analog circuits.

17. The semiconductor integrated circuit according to claim 16, wherein:

the digital circuit further has a MOS transistor having a gate connected to the first external terminal; and

the fuse element has a resistance value that satisfies:

$$V_{OX} > (R_m + R_x) \times I_{esd}$$

where V_{OX} represents a breakdown voltage of a gate oxide film of the MOS transistor, R_m represents a wire resistance value in the electrostatic discharge current path between the first and second external terminals, R_x represents a resistance value of the fuse element, and I_{esd} represents a value of an electrostatic discharge current.

18. The semiconductor integrated circuit according to claim 16, wherein the fuse element remains firm even when energy of 200μJ is applied thereto.

19. The semiconductor integrated circuit according to claim 16, wherein the fuse element remains firm even

when energy of 200μJ is applied thereto but breaks when a direct current of 30mA is applied thereto within 20 seconds.

20. The semiconductor integrated circuit according to claim 16, wherein the fuse element is electrically disconnected when the semiconductor integrated circuit is mounted on a circuit board.